SECURE-IC
THE SECURITY SCIENCE COMPANY

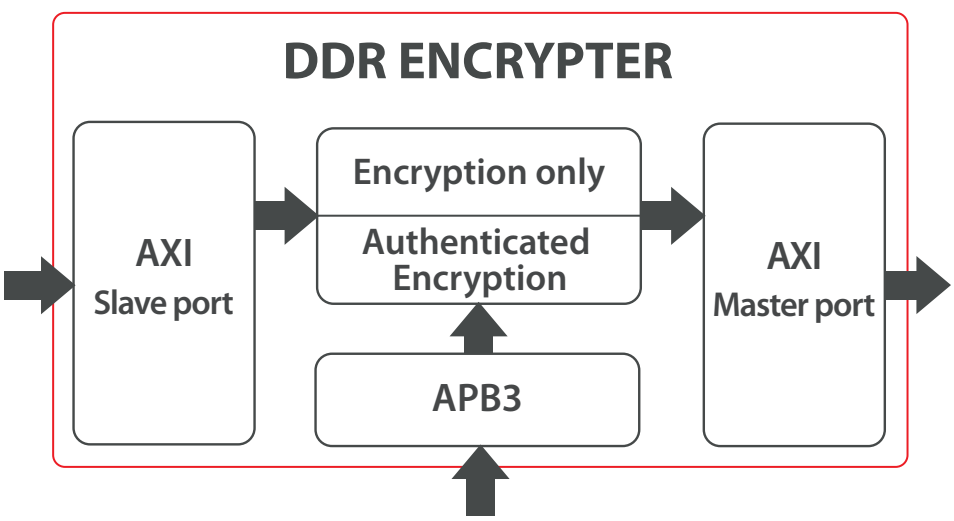
PRODUCT SHEET

Securyzr™ > Securyzr™ Secure HW Solutions > Securyzr™ Security IP > Tunable Crypto > Memory Protection > SCZ_IP_MP_DDRenc

DDR ENCRYPTER

The DDR encrypter IP Core module enables on-the-fly encryption and authentication to the external memory.

It supports AXI slave/master interfaces, APB port for configuration purpose. It is typically placed between the processor(s) and an external memory controller (DDRx). This IP Core improves tamper resistance by avoiding any modification, spoofing or analysis of external data.



Features

- Protects the external memory
- On-the-fly encryption
- Optional authentication
- Transparent for the processor
- Scalable data bus width
- AMBA Master/Slave interfaces
- Multi-region management
- Scalable throughput
- ASIC and FPGA (incl. UltraScale+ & Versal)

Applications

- Defence
- Data Center
- Payment

Implementation aspects

The processor can securely and transparently write/read data or code from external memory. It leverages the AES Core from Secure-IC. The unique architecture enables a high level of flexibility and allows it to be used by microcontroller and multi-core architectures. The features required by a specific application can be taken into account in order to select the most optimal configuration for any FPGA or ASIC technology.

Deliverables

- Netlist or RTL
- Scripts for synthesis & STA
- Self-checking RTL test-bench on referenced vectors
- Documentation

V4.0

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